Notice of Allowability	Application No.	Applicant(s)	
	09/682,188	UEDA, MAKOTO	
	Examiner	Art Unit	
	Kenneth Tang	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/11/06*.

2. ☒ The allowed claim(s) is/are *1,3-9,12-15 and 18-20; now renumbered as 1-15*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☒ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *3/28/06* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SUPERVISORY PATENT

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Frank V. DeRosa (Reg. No. 43,584) on 3/28/06.

3. Please amend the claims according to the email attachment sent by the Applicant on 3/28/06.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt
3/28/06

SUPERVISORY PATENT EXAMINER

Requested by Examiner 3/28/06 KT

Tang, Kenneth

From: Frank V. DeRosa, Esq. (F.Chau&Associates LLC) [derosa@chauiplaw.com]
Sent: Tuesday, March 28, 2006 2:07 PM
To: Tang, Kenneth
Subject: re: U.S. Serial No. 09/682,188

Examiner Tang:

As we discussed, attached is a Supplemental Amendment to place the application in condition for allowance. If you have any questions or comments, please feel free to contact me.

Regards,
****

Frank V. DeRosa, Esq.
F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, New York 11797
Tel: (516) 692-8888
Fax: (516) 692-8889

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Ueda et al.	**Examiner:** K. Tang	
Serial No:	09/682,188	**Group**: Art Unit 2195	
Filed:	August 2, 2001	**Docket:** JP920000046US1 (8728-728)	

For: **MULTIPROCESSOR SYSTEM, PROCESSOR MODULE FOR USE THEREIN, AND TASK ALLOCATION METHOD IN MULTIPROCESSING**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

This is a Supplemental Amendment to the Applicants' Amendment Filed on January 11, 2006. Please amend the claims as follows:

Listing of Claims

1. (Currently Amended) In multiprocessing, which is performed by using a plurality of processor modules, each of the plurality of processor modules including a cache memory and a plurality of processors sharing the cache memory, a method of allocating a task to each processor comprising the steps of:

monitoring access conditions of respective tasks to data shared among cache memories in the processor modules; and

allocating tasks that make frequent accesses to the same shared data to processors in the same module, on the basis of said access conditions;

wherein said step of monitoring access conditions comprises the substeps of:

detecting an update to the shared data stored in a cache memory in one of the processor modules, said update causing an invalidation of the shared data stored in the cache memories in the other processor modules; and

storing identification information of tasks that caused said invalidation, and an address of the updated data, and the number of invalidations of the same data by the same task; and

wherein said step of allocating tasks comprises the substeps of:

classifying tasks into groups on the basis of the number of invalidations of the same data; and

allocating tasks in the same group to respective processors in the same processor module.

2. (Canceled)

3. (Currently Amended) ~~The method according to claim 1,~~ In multiprocessing, which is performed by using a plurality of processor modules, each of the plurality of processor modules including a cache memory and a plurality of processors sharing the cache memory, a method of allocating a task to each processor comprising the steps of:

monitoring access conditions of respective tasks to data shared among cache memories in the processor modules; and

allocating tasks that make frequent accesses to the same shared data to processors in the same module, on the basis of said access conditions;

wherein said step of monitoring access conditions comprises the substeps of:

detecting and storing an update to the shared data stored in one of the cache memories, said update causing an invalidation of the shared data stored in the other cache memories; and

monitoring access conditions of respective tasks to the invalidated data, and

wherein said step of allocating tasks comprises:

classifying tasks into groups on the basis of the number of invalidations of the same data; and

allocating tasks in the same group to respective processors in the same processor module.

4. (Original): The method according to claim 3, wherein said substep of monitoring access conditions comprises:

detecting an access to the invalidated data; and

storing an address of the invalidated data, identification information of a task that accessed the invalidated data, and the number of accesses to the same shared data by the same task.

5. (Original): The method according to claim 4, wherein said detecting an access to the invalidated data comprises: detecting an invalidation of data; storing an address of the invalidated data; detecting a cache miss; comparing an address of the data that caused the cache miss with the stored address of the invalidated data.

6. (Currently Amended): The method according to claim 1 [2], further comprising the step of: making a request for allocation of tasks to an operating system performing multiprocessing, when the total number of said stored invalidations or said accesses exceeds a predetermined value.

7. (Original): The method according to claim 4, further comprising the step of: making a request for allocation of tasks to an operating system performing multiprocessing, when the total number of said stored invalidations or said accesses exceeds a predetermined value.

8. (Original): The method according to claim 5, further comprising the step of: making a request for allocation of tasks to an operating system performing multiprocessing, when the total number of said stored invalidations or said accesses exceeds a predetermined value.

9. (Currently Amended) A multiprocessor system, in which a plurality of processor modules, each of the plurality of processor modules including one cache memory and a plurality of processors sharing the cache memory are used, comprising:

~~(a)~~ a plurality of processor modules including:

a detector for detecting accesses by respective tasks to data shared among cache memories in the processor modules; and

a storage device for storing an address of the shared data, identification information of the tasks that accessed the shared data, and the number of accesses to the same shared data by the same task; and

~~(b)~~ an allocator for allocating tasks that make frequent accesses to the same shared data to processors in the same module, on the basis of the number of accesses;

wherein said detector for detecting accesses comprises:

a first device for detecting an update to the shared data stored in a cache memory in one of the processor modules, said update causing an invalidation of the shared data stored in the cache memories in the other processor modules; and

a second device for storing identification information of a task that caused said invalidation, and an address of the updated data, and the number of invalidations of the same data by the same task.

10. (Canceled)

11. (Canceled)

12. (Currently Amended) ~~The multiprocessor system according to claim 11,~~ A multiprocessor system, in which a plurality of processor modules, each of the plurality of processor modules including one cache memory and a plurality of processors sharing the cache memory are used, comprising:

a plurality of processor modules including:

a detector for detecting accesses by respective tasks to data shared among cache memories in the processor modules, and

a storage device for storing an address of the shared data; identification information of the tasks that accessed the shared data, and the number of accesses to the same shared data by the same task; and

an allocator for allocating tasks that make frequent accesses to the same shared data to processors in the same module, on the basis of the number of accesses;

wherein said detector for detecting accesses comprises:

a first device for detecting and storing an update to the shared data stored in one of a plurality of cache memories, said update causing an invalidation of the shared data stored in the other cache memories; and

an access detector for detecting accesses to the invalidated data by respective tasks;

wherein said first device for detecting and storing an update to the shared data comprises:

invalidation means for detecting an invalidation of data; and

first address means for storing an address of the invalidated data; and

wherein said access detector for detecting accesses comprises:

cache detector means for detecting a cache miss; and

second address means for comparing an address of the data that caused the cache miss with the stored address of the invalidated data.

13. (Original) The multiprocessor system according to claim 9, further comprising: request means for making a request for allocation of tasks to said allocator for allocating tasks, when the total number of said stored invalidations or said accesses exceeds a predetermined value.

14. (Currently Amended) The multiprocessor system according to claim 9 [10], further comprising: request means for making a request for allocation of tasks to said allocator for allocating tasks, when the total number of said stored invalidations or said accesses exceeds a predetermined value.

15. (Currently Amended) A plurality of processor modules for use in a multiprocessor system, each of the plurality of processor modules including a cache memory and a plurality of processors sharing the cache memory, comprising:

a detector for detecting accesses by respective tasks to data shared among cache memories in the processor modules; and

a storage device for storing an address of the shared data, identification information of the tasks that accessed the shared data, and the number of accesses to the same shared data by the same task;

wherein said detector for detecting accesses comprises:

a first device for detecting an update to the shared data stored in a cache memory in one of the processor modules, said update causing an invalidation of the shared data stored in the cache memories in the other processor modules; and

a second device for storing identification information of a task that caused said invalidation, and an address of the updated data, and the number of invalidations of the same data by the same task.

16. (Canceled)

17. (Canceled)

18. (Currently Amended) ~~The plurality of processor modules according to claim 17,~~ A plurality of processor modules for use in a multiprocessor system, each of the plurality of processor modules including a cache memory and a plurality of processors sharing the cache memory, comprising:

a detector for detecting accesses by respective tasks to data shared among cache memories in the processor modules; and

a storage device for storing an address of the shared data, identification information of the tasks that accessed the shared data, and the number of accesses to the same shared data by the same task;

wherein said means for detecting accesses comprises:

a first device for detecting and storing an update to the shared data stored in one of the cache memories, said update causing an invalidation of the shared data stored in the other cache memories; and

an access detector for detecting accesses to the invalidated data by respective tasks; and

wherein said means for detecting and storing an update to the shared data comprises:

invalidation means for detecting an invalidation of data; and

first address means for storing an address of the invalidated data; and

wherein said access detector for detecting accesses comprises:

cache detector means for detecting a cache miss; and

second address means for comparing an address of the data that caused the cache miss with the stored address of the invalidated data.

19. (Previously Presented) The plurality of processor modules according to claim 12, further comprising: request means for making a request for allocation of tasks to an operating system performing multiprocessing, when the total number of said stored invalidations or said accesses exceeds a predetermined value.

20. (Currently Amended) The plurality of processor modules according to claim 15 ~~16~~, further comprising: request means for making a request for allocation of tasks to an operating system performing multiprocessing, when the total number of said stored invalidations or said accesses exceeds a predetermined value.

21. (Canceled)

REMARKS

This Amendment is being made in view of the Examiner's indication that claims 2, 3, 10, 12, 16, and 18 would be allowable if rewritten in independent form. Although Applicants respectfully disagree with the claim rejections for at least claims 1, 9, 15, and 21 for reasons previously explained, the claims have been amended solely for the purpose of expediting prosecution and placing the application in condition for allowance.

For instance, by the above amendment, claim 1 has been amended to include the subject matter of canceled claim 2. Claim 3 has been rewritten in independent form to include the subject matter of claim 1. Claim 9 has been amended to include the subject matter of canceled claim 10. Claim 12 has been rewritten in independent form to include the subject matter of claim 9 and canceled claim 11. Claim 15 has been amended to include the subject matter of canceled claim 16. Claim 18 has been rewritten in independent form to include the subject matter of claim 15 and canceled claim 17. Claim 21 has been canceled without prejudice. Moreover, claims 6, 14 and 20 have been amended to change their dependency as appropriate.

In view of the foregoing, it is believed that that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

/Frank DeRosa/
Frank V. DeRosa
Reg. No. 43,584
Attorney for Applicants

F.CHAU & ASSOCIATES, LLC
130 Woodbury Road
Woodbury, NY 11797
Telephone: (516) 692-8888
Facsimile: (516) 692-8889